Course Curriculum

for

Master of Technology Programme

in

Electronics and Communication Engineering Department

National Institute of Technology Goa

Farmagudi, Ponda, Goa - 403 401

Semester-wise Credit Distribution

Semester	Total Credits
I	19
II	17
III	14
IV	14
Total Credits	**64**

M.Tech. Program Name: VLSI

Semester-wise Distribution of the Courses

Semester I				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1	EC600	Digital IC Design	(3-0-0)	3
2	EC601	Analog IC Design	(3-0-0)	3
3	EC602	Semiconductor Device Theory and Modelling	(3-0-0)	3
4	EC603	Digital Signal Processing	(3-0-0)	3
5	EC604	IC Design Laboratory	(0-0-6)	3
6	EC605	Semiconductor Device Simulation Laboratory	(0-0-3)	2
7	EC606	Seminar	(0-0-3)	2
Total Credits				**19**

Semester II				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1	EC650	VLSI Testing and Testability	(3-0-0)	3
2	EC651	VLSI Technology	(3-0-0)	3
3		Elective I	(3-0-0)	3
4		Elective II	(3-0-0)	3
5	EC652	System Design Laboratory	(0-0-6)	3
6	EC653	VIVA-VOCE	-	2
7	HU650*	Communication Skills and Technical Writing	(1-0-2)	-
Total Credits				**17**

Semester III				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1		Elective III	(3-0-0)	3
2		Elective IV	(3-0-0)	3
3	EC700	Major Project-I	(0-0-12)	8
Total Credits				**14**

Semester IV				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1	EC750	Major Project-II	(0-0-21)	14
Total Credits				**14**

List of Electives

Electives				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1	EC800	Optoelectronics and Photonics	(3-0-0)	3
2	EC801	Architectural Design of IC	(3-0-0)	3
4	EC802	Digital Design using FPGA	(3-0-0)	3
5	EC803	System on CHIP	(3-0-0)	3
6	EC804	Mixed Signal Design	(3-0-0)	3
7	EC805	VLSI Embedded Systems	(3-0-0)	3
8	EC806	VLSI Design Automation	(3-0-0)	3
9	EC807	Compound Semiconductor Devices	(3-0-0)	3
10	EC808	Nano-electronic Device Engineering	(3-0-0)	3
11	EC809	Active Filter Design	(3-0-0)	3
12	EC810	Low Power VLSI Design	(3-0-0)	3
13	EC811	Power Management IC's	(3-0-0)	3
14	EC812	Advanced Topics in VLSI	(3-0-0)	3
15	EC813	Memory Design & Testing	(3-0-0)	3
16	EC814	IC for Broadband communication	(3-0-0)	3
17	EC815	CMOS RF IC Design	(3-0-0)	3
18	EC816	Advanced Antenna Theory	(3-0-0)	3
19	EC817	VLSI Signal Processing	(3-0-0)	3
20	EC818	Multi-rate Signal Processing	(3-0-0)	3
21	EC819	Multimedia Systems	(3-0-0)	3
22	EC820	Selected Topics in ECE - I		1
23	EC821	Selected Topics in ECE - II		2
24	EC822	Selected Topics in ECE - III	(3-0-0)	3

Program Electives				
SI. No.	**Course Code**	**Course Name**	**Total Credits** (L-T-P)	**Credits**
1	EC850	Data Structures and Algorithms	(3-0-0)	3
2	EC851	Advanced Computer Architecture	(3-0-0)	3
3	EC852	Optimization Techniques	(3-0-0)	3
4	EC853	Linear Algebra	(3-0-0)	3
5	EC854	Random Processes	(3-0-0)	3

Core Subject Syllabus

<table>
<tr><td>Subject Code

EC600</td><td colspan="2">Digital IC Design</td><td>Credits: 3(3-0-0)

Total hours: 42</td></tr>
<tr><td>Course Objectives</td><td colspan="3">To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles. The course also involves analysis of performance metrics.</td></tr>
<tr><td>Module 1</td><td colspan="2">Implementation of strategies for digital ICs</td><td>10 hours</td></tr>
<tr><td colspan="4">Custom Circuit design, Cell based and Array based design implementations. Static and Dynamic Characteristics of CMOs inverter, Power dissipation, Logical effort.</td></tr>
<tr><td>Module 2</td><td colspan="2">Designing combinational and sequential circuits</td><td>14 hours</td></tr>
<tr><td colspan="4">Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and dynamic properties of complex gates, Dynamic CMOS Logic. Timing metrics of sequential circuits, Dynamic latches and Registers. Pipelining.</td></tr>
<tr><td>Module 3</td><td colspan="2">Interconnect and Timing Issues</td><td>12 hours</td></tr>
<tr><td colspan="4">Circuit characterization and performance estimation - Resistance, Capacitance
estimation - Switching characteristics - Delay models –Timing issues in Digital circuits, Power dissipation. Impact of Clock Skew and Jitter.</td></tr>
<tr><td>Module 4</td><td colspan="2">Memory Design</td><td>6 hours</td></tr>
<tr><td colspan="4">Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.</td></tr>
<tr><td colspan="4">Reference Books

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic Digital Integrated Circuits - A design perspective, Pearson, 2003.
2. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, McGraw Hill, 1999.
3. John P. Uyemura, Introduction to VLSI Circuits, Wiley India Pvt. Ltd., 2012.
4. Eugene Fabricius, Introduction to VLSI Design, New Ed Edition, Tata McGraw - Hill Education, 1990.
5. Material from the Journal of Solid-state Circuits and the International Solid-state Circuits Conference proceedings.</td></tr>
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Subject Code **EC601**	**Analog IC Design**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the analysis and design of analog integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.	
Module 1	**CMOS amplifiers basics**	12 hours
Introduction to MOS Capacitances, passive components and their parasitics, small and large signal modelling and analysis. Different Single stage and Differential Amplifiers, Current Mirrors.		
Module 2	**Multi-stage amplifiers**	12 hours
Telescopic and Folded cascode amplifiers, Slew-rate, Pole splitting, Two-stage amplifiers - analysis, Frequency response, Stability compensation, Common mode feedback analysis, feedback amplifier topologies.		
Module 3	**References**	6 hours
Supply independent biasing, Bandgap reference, Constant-Gm biasing.		
Module 4	**Nonlinearity, Mismatch and Layout**	10 hours
Noise: Types of Noise, noise model, Nonlinearity of Differential Circuits, Capacitor nonlinearity, Mismatch analysis, Offset cancellation techniques, Layout Techniques		

Reference Books

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Mcgraw-Hill Education, 2002.
2. David Johns & Ken Martin, *Analog Integrated Circuit Design*, Wiley-India, 2008.
3. P. Allen & D. R. Holberg, *CMOS Analog Circuit Design*, Oxford Press, 2011.
4. P. Gray, P. Hurst, S. Lewis, R. Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley-India, 2008.
5. Gregorian and Temes, Analog MOS Integrated Circuits for Signal Processing, Wiley-India, 2008.

Subject Code EC602	Semiconductor Device Theory and Modelling	Credits: 3(3-0-0) Total hours: 42
Course Objectives	To familiarize with the physical concepts behind the operation of microelectronic devices and also covers high performance, high speed semiconductor devices used in VLSI systems.	
Module 1	**Concentration and motion of carriers in Semiconductor bulk**	8 hours
Valence band and Energy band models of intrinsic and extrinsic semiconductors. Thermal equilibrium carrier concentration. Carrier transport phenomena, Recombination and generation.		
Module 2	**Quantitative theory of PN junctions**	10 hours
Band diagrams, electrostatics of a p-n junction diode, ideal static I-V characteristics and deviations including breakdown, ac small signal equivalent circuit, switching characteristics, Schottky junctions, Ohmic contacts.		
Module 3	**BJT**	10 hours
Bipolar device Design and Modeling, Small and large signal models, Non-ideal effects, breakdown voltage, charge storage, Multidimensional effects, Bipolar Device optimization & performance factors for digital and analog circuits, Brief overview of BJT CAD SPICE model and VBIC model introduction.		
Module 4	**MOSFET Alternate MOS structures**	14 hours
Analysis of MOSFET, Calculation of threshold voltage. Static I-V characteristics of MOSFETs, MOSFET capacitances, C-V characteristics, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET models for calculation, Alternate MOS structures (SOI devices and Multi-gate MOSFETs) in brief.		

Reference Books

1. M. S. Tyagi, *Introduction to Semiconductor materials and Devices*, John Wiley & Sons, 1991.
2. S. M. Sze, *Modern Semiconductor Device Physics*, Wiley, 1998.
3. Yuan Taur & Tak H Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.
4. Ben G. Streetman, *Solid State Electronic Devices*, Prentice Hall, Fifth Edition, 2000.
5. J. P. Colinge, FinFETs and other multigate transistors, Springer, 2007.

Subject Code **EC603**	**Digital Signal Processing**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	To expose to the basic concepts in digital processing system design with emphasis on the digital filter design and related algorithmic and implementation issues. Specifically, focus will be on FIR, IIR Filters classical and optimized design techniques, issues related to finite word length and advantage of specific structures for implementation. Various specific digital filters will be discussed and their use for some signal processing applications will be also discussed.	
Module 1	**Review of Signals and Systems**	8 hours
Introduction to CT signals and systems, DT signals and systems, Frequency analysis of signals, Transform domain analysis of LTI systems, DFT- Properties, FFT algorithms.		
Module 2	**Design of Digital Filters**	12 hours
Digital filter structures, IIR Digital filter design and implementation, FIR digital filter design and implementation, Digital filter applications, Optimization Techniques in Filter Design.		
Module 3	**Finite Word length problems in Digital Filters**	12 hours
Representation of binary numbers in digital filters, Fixed and Floating point representation, Error due to quantization, truncation and round off, Implementation of different structures, Issues associated with IIR filters.		
Module 4	**Introduction to Multi-rate Signal Processing**	10 hours
Sampling rate conversion, Decimation by an integer factor, Interpolation by an integer factor, Sampling rate conversion by a rational factor, Sampling rate converter as a time variant system, Practical structures for decimators and interpolators. Multi stage implantation of digital filters.		

Reference Books

1. John G. Proakis, and Dimitris G. Manolakis, *Digital Signal Processing Principles, Algorithms and Applications,* Pearson, 2002.
2. P.S.R. Diniz, E. A. B. da Silva, and S. L. Netto, *Digital Signal Processing System Analysis and Design*, Cambridge, 2010.
3. Sanjit K. Mitra,*Digital Signal Processing A Computer-Based Approach,* McGraw Hill, 2003.
4. Vinay K. Ingle and John G. Proakis, *Essential of Digital Signal Processing using MATLAB,* Cengage Learning, 2012.
5. P. P. Vaidyanathan, *Multirate Systems and Filter Banks*, Pearson-Education, Delhi, 2004.
6. N. J. Fliege N J, *Multirate Digital Signal Processing*, John Wiley and sons, 1994.

Subject Code **EC604**	**IC Design Laboratory**	Credits:3 (0-0-6) Total hours: 84
Course Objectives	This course introduces CMOS schematic design, layout techniques, automated design tools, netlist synthesis, place & route and timing verification. EDA Tools will be introduced in this course.	
Module 1	**Digital IC design**	
Schematic simulation of CMOS Inverter, power and delay issues and Layout techniques. Pre layout simulation, Parasitic extraction, Post layout simulation. Design of Adders, Multiplier and Shifters, Synthesis with timing constraints, Pre layout simulation, Floor planning, Placement, Routing, Parasitic extraction, Post layout simulation. Standard cell layout techniques.		
Module 2	**Analog IC design**	
Single stage amplifiers: Completer characterization of Common source amplifier, Common drain amplifiers, Common Gate amplifiers, Cascode amplifiers. Differential amplifiers: Completer characterization of Single stage differential amplifiers, Folded Cascode, Telescopic amplifiers Two-stage amplifiers. Layout techniques		
Reference Books 1. James R.Armstrong, F.Gail Gray, *VHDL Design Representation and Synthesis*, Pearson Education, 2007. 2. Jan M Rabaey, *Digital Integrated Circuits - A Design Perspective*, Prentice Hall, Second Edition, 2005. 3. Naveed A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Springer, Third Edition,1999. 4. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education, 2002. 5. Allan Hastings**,** *The Art of Analog Layout*, Prentice Hall, Second Edition, 2005.		

Subject Code **EC605**	**Semiconductor Device Simulation Laboratory**	Credits: 2 (0-0-3) Total hours: 42
Course Objectives	This course covers the analysis and design of pn diode, BJT, MOSFET and novel device structures.	
Module 1	**2D simulations**	
Use device simulator to generate a pn diode structure. Simulate I-V characteristics and also get the C-V characteristics. Find the carrier concentration, electron and hole concentration, electric field, potential distribution (at different biases) and doping distribution across the structure. Check the current and capacitance values with hand calculations. Extract Vbi from capacitance characteristics. Freeze different models one used. Process simulates the same structure with same/similar doping levels. Exporting the process simulated structure in to device simulator, extract I-V and C-V characteristics and make similar observations as in device simulation and explain the differences if any.		
Module 2	**BJT simulations**	
Bipolar devices are integral part of high speed circuit. Any given MOSFET has a parasitic BJT. If not taken care in device design, the parasitic BJT may lead to very different behavior. The aim of these experiments is to understand the different effects in BJT. For a lateral/planar BJT, the following experiments can be performed: 1) Variation in α, βdc and γ with base doping and base width and respective current characteristics 2) Variation in α, βdc and γ with emitter width and respective current characteristics		
Module 3	**3D MOS device**	
Simulate a 3D MOS device (FINFET/SOI/Piller MOSFET, Tri-gate MOSFET GAA MOSFET) and obtain their characteristics.		
Reference Books 1. User Manuals of respective software. 2. Jean- Pierrie Colinge, *Silicon-on-insulator Technology: Materials to VLSI*, Springer, Second Edition, 1997. 3. M.S. Tyagi, *Introduction to Semiconductor materials and Devices*, John Wiley & Sons, 1991. 4. J. P. Colinge, *FinFETs and other multigate transistors*, Springer, 2007.		

Subject Code **EC650**	**VLSI Testing and Testability**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	This course covers introduction to the concepts and techniques of VLSI (Very Large Scale Integration) design verification and testing. Details of test economy, fault modeling and simulation, defects, Automatic Test Pattern Generation (ATPG), design for testability, and built-in self-test (BIST) also covered.	
Module 1	**Fundamental of VLSI testing**	12 hours
Basic of VLSI testing, Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs.		
Module 2	**Fault Modeling and testing**	12 hours
Fault models, fault detection and redundancy, fault equivalence and fault location, fault dominance, automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan. System testing and test for SOCs. Delay fault testing.		
Module 3	**Test automation and Design verification**	10 hours
BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches.		
Module 4	**Functional and Timing verification**	8 hours
Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.		

Reference Books

1. M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, Jaico Publishing House, 1990.
2. T. Kropf, *Introduction to Formal Hardware Verification*, Springer Verlag, 2000.
3. Neil H. E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley, Second Edition, 1993.
4. Neil H. E. Weste and David Harris, *Principles of CMOS VLSI Design*, Addison Wesley, Third Edition, 2004.
5. M. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.

Subject Code **EC651**	**VLSI Technology**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.	
Module 1	**Crystal Growth, Wafer manufacturing and Clean rooms**	12 hours
CMOS Process flow starting from Substrate selection to multilevel metal formation, comparison between bulk and SOI CMOS technologies. Crystal structure, Czochralski and FZ growth methods, Wafer preparation and specifications, SOI Wafer manufacturing. **Clean rooms, wafer cleaning and gettering**: Basic concepts, manufacturing methods and equipment, Measurement methods.		
Module 2	**Photolithography and Oxidation**	10 hours
Photolithography: Light sources, Wafer exposure systems, Photoresists, Baking and development, Mask making, Measurement of mask features and defects, resist patterns and etched features. **Oxidation:** Wet and Dry oxidation, growth kinetics and models, defects, measurement methods and characterization.		
Module 3	**Diffusion and Ion-implantation**	8 hours
Diffusion: Models for diffused layers, Characterization methods, Segregation, Interfacial dopant pileup, oxidation enhanced diffusion, dopant-defect interaction. **Ion-implantation**: Basic concepts, High energy and ultralow energy implantation, shallow junction formation & modeling, Electronic stopping, Damage production and annealing, RTA Process & dopant activation		
Module 4	**Thin film Deposition, Etching Technologies and Back-end Technology**	12 hours
Thinfilm Deposition: Chemical and physical vapour deposition, epitaxial growth, manufacturing methods and systems, deposition of dielectrics and metals commonly used in VLSI, Modeling deposition processes. **Etching Technologies:** Wet etching, Plasma etching, RIE, Etching of materials used in VLSI, Modeling of etching. **Back-end Technology:** Contacts, Vias, Multi-level Interconnects, Silicided gates and S/D regions, Reflow & planarization, Multi-chip modules and packaging.		

Reference Books

1. James Plummer, M. Deal and P.Griffin, *Silicon VLSI Technology*, Prentice Hall Electronics, 2000.
2. Stephen Campbell, *The Science and Engineering of Microelectronics*, Oxford University Press, 1996.
3. S. M. Sze (Ed), *VLSI Technology*, McGraw Hill, Second Edition, 1988.
4. S.K. Ghandhi, *VLSI Fabrication Principles*, John Wiley Inc., New York, 1983.
5. C.Y. Chang and S. M. Sze (Ed), *ULSI Technology*, McGraw Hill Companies Inc, 1996.

Subject Code **EC652**	**System Design Laboratory**	Credits:3 (0-0-6) Total hours: 84
Course Objectives	This course covers the Laboratory topics based on the core and elective subjects. Example syllabus based on electives like System on chip or CMOS RF IC is given below. a) **System on chip lab** course introduces CAD tool for system design and implementation of Prototype SoC platform using FPGA and ARM processor boards. Xilinx ISE, EDK and ARM tool-chain will be used in this course. b) The objective of this course is to cover the design issue related to **RF IC Design**.	
Module 1	**System on chip**	
Development of embedded systems in both ARM and FPGA platforms. Examples on multiprocessor environments. Application case studies of signal processing applications FFT, FIR, DCT, JPEG, H.264 etc. Custom IP interfacing techniques for different protocols for above applications. Embedded OS development on FPGA/ARM platforms and device driver development. Mini Project		
Module 2	**RF IC Design**	
Characterization of a MOS transistor for RF, Design of a tuned LNA and performance analysis, Design of a VCO and performance analysis, Design of a mixer based on a Gilbert cell. Mini Lab Projects		

Reference Books:

1. Doug Amos, Austin Lesea and Rene Richter, *FPGA-Based Prototyping Methodology Manual Best Practices in Design-for-Prototyping*, Synopsys, Inc, Mountain View, 2010.
2. Ron Sass and Andrew G. Schmidt, *Embedded Systems Design with Platform FPGAs Principles and Practices*, Elsevier Inc, 2010.
3. J. Staunstrup and W. Wolf, *Data books of ARM7/ARM9*, *Hardware/Software Co-Design: Principles and Practice*, Kluwer Academic Publishers, 1997.
4. Silage, Dennis, *Embedded Design Using Programmable Gate Arrays*, Book stand Publishing, 2008.
5. K.V.K.K. Prasad, *Embedded Real Time Systems: Concepts, Design & Programming*, Dreamtech Publication, 2003.
6. G. DeMicheli, R. Ernst, and W. Wolf, *Readings in Hardware/Software Co-Design*, Academic Press, 2002.
7. *User manual of the tools for RF IC design.*
8. Razavi, B., *RF microelectronics.2nd ed. int.* Pearson Education International, 2012.
9. Lee, T.H., *The design of CMOS radio-frequency integrated circuits*. 2nd ed. Cambridge: Cambridge University Press, 2004.

Subject Code **EC606**	**Seminar**	**Credits: 2 (0-0-3)**
Course Objectives	Students will have to choose a topic in current VLSI related areas or industry practices and prepare a write up along with suitable presentation and demonstration.	

Subject Code **EC653**	**VIVA-VOCE**	**Credits: 2**
Course Objectives	Students will have to attend for a viva-voce in front of all the faculty of the department for the evaluation of the subjects studied in the first year (I and II semesters) with a suitable demonstration.	

Subject Code **HU650* (Audit Course)**	**Communication Skills and Technical Writing**	Credits: 0 (1-0-2) Total hours: 45
Course Objectives	This course is meant for developing Professional Communication and Technical Writing Skills among the students. The Lab hours will give emphasis on Technical Presentation and Seminar (on different emerging topics) followed by question-answer and discussion.	
Module 1		12 hours
Introduction to Communication-Definition-Types-Classifications, Writing Exercises-Paragraph- Précis-Summary/Executive Summary/Abstract		
Module 2		8 hours
Technical Reports-Types-Format-Nuances to be followed		
Module 3		10 hours
Preparation of Technical Document-Reports-Instruction Manuals-Project Proposal (Prefatory Part- Main Part-Terminal Section)		
Module 4		15 hours
Presentation of Technical Report (Kinesics, Proxemics, and Professional Ethics)		
Reference Books 1. Raman and Sharma, *Communication Skills*, OUP, 2011. 2. Mandel, Steve, *Technical Presentation Skills: A Practical Guide for Better Speaking* (Revised Edition), Crisp Learning, 2000. 3. Wood, Millett, *The Art of Speaking*, Drake Publishers, 1971. 4. Lencioni, Patrick, *The Five Dysfunctions of a Team*, John Wiley and Sons, 2006.		

Subject Code **EC800**	**Optoelectronics and Photonics**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course will cover basic laser theory, semiconductor physics, optical properties of semiconductors and quantum wells, optical detection and noises, electromagnetic waves. The primary emphasis will be on semiconductor materials and devices.	
Module 1	**Semiconductor lasers**	10 hours
Semiconductor lasers for optical fiber communications, Fabry-Perot cavity, heterostructure semiconductor lasers, single frequency semiconductor lasers, semiconductor lasers for coherent systems. Distributed feedback in Ga-As-P lasers.		
Module 2	**Photo detectors and Optical Receiver Operation**	12 hours
Device structure and fabrication, photo-detectors for fiber optics, reverse bias photo-detectors, dark current, quantum efficiency, signal to notice ratio, types of detectors. Receivers for digital fiber optic communication systems: basic components, detectors for digital fiber optic receivers, PIN diode, Avalanche photodiode, Fronts ends for digital fiber optic receivers, equalizer for optical communication, receivers, PIN-FET receivers for longer wavelength communication systems.		
Module 3	**Transmission System**	12 hours
Coherent optical fiber transmission systems, coherent detection principles, comparison of direct and coherent performance, homodyne and heterodyne systems. Nonlinear process in optical fibers, phase matching in waveguide, phase matched harmonic generation in waveguides. Second harmonic generation (SHG) in integrated optics, Cerenkov configuration SHG.		
Module 4	**Sensor and Devices**	8 hours
Optical fiber sensor and devices, intensity modulation through light interruption, distributed sensing with fiber optics. Basic principles of interferometric optical fiber sensor, signal processing in mono mode fiber optic sensor, photonic band gap materials.		

Reference Books

1. G. Keiser, *Optical fiber communication*, McGraw-Hill, 2008.
2. J. Seniar, *Optical fiber Communication*, Prentice-Hall International, 1985.
3. A. K. Ghatak, *Introduction to optical fiber*, Cambridge University Press, 1998.
4. Max Born & Emil Wolf, *Principles of Optics*, Cambridge University Press, 1999.
5. Saleh & Teich, *Fundamentals of Photonics*, Wiley-Interscience, 2007.

Subject Code **EC801**	**Architectural Design of ICs**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers algorithm, architecture and circuit design trade-offs to optimize for power, performance and area.	
Module 1		12 hours
VLSI Design flow, general design methodologies, Mapping algorithms into Architectures: Signal flow graph, data dependences, data-path synthesis, control structures, critical path and worst case timing analysis, concept of hierarchical system design; Data-path element: Data-path design philosophies, fast adder, multiplier, driver etc.		
Module 2		12 hours
Data-path optimization, application specific combinatorial and sequential circuit design, CORDIC unit; Pipeline and parallel architectures: Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures; Control strategies: Hardware implementation of various control structures, micro-programmed control techniques, VLIW architecture		
Module 3		10 hours
Testable architecture: Controllability and observability, boundary scan and other such techniques, identifying fault locations, self-reconfigurable fault tolerant structures.		
Module 4		8 hours
Trade-off issues: Optimization with regard to speed, area and power, asynchronous and low power system design, ASIC (application specific integrated circuits) and ASISP (application specific instruction set processors) design		

Reference Books

1. U. Meyer-Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, Springer-Verlag, 2001.
2. S. Y. Kung, *VLSI Array Processors.Prentice*, Prentice-Hall, 1988.
3. K. Parhi, *VLSI Digital Signal Processing Systems*, Wiley & Sons, 1999.
4. J. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, Second Edition, 2003.

Subject Code **EC802**	**Digital Design using FPGAs**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	To learn field programmable gate array (FPGA) technologies and utilize associated computer aided design (CAD) tools. To synthesize digital systems with testing strategies and construct test benches.	
Module 1	**Introduction**	08 hours
Digital system design options and trade-offs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioural modelling and simulation.		
Module 2	**Tool for logic Implementation**	12 hours
Hardware description languages, combinational and sequential design, state machine design, synthesis issues, test benches. Overview of FPGA architectures and technologies: FPGA Architectural options, granularity of function and wiring resources, coarse vs fine grained, vendor specific issues (emphasis on Xilinx / Altera).		
Module 3	**Implementation on FPGA**	12 hours
Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation, Programmable interconnect - Partitioning and Placement, Routing resources, delays.		
Module 4	**Applications**	10 hours
Applications - Embedded system design using FPGAs, DSP using FPGAs, Dynamic architecture using FPGAs, reconfigurable systems, application case studies. Simulation / implementation exercises of combinational, sequential and DSP kernels on Xilinx / Altera boards.		
Reference Books 1. M. J. S. Smith, *Application Specific Integrated Circuits*, Pearson, 2000. 2. Peter Ashenden, *Digital Design using Verilog*, Elsevier, 2007. 3. W. Wolf, *FPGA based system design*, Pearson, 2004. 4. Clive Maxfield, *The Design Warriors's Guide to FPGAs*, Elsevier, 2004.		

Subject Code **EC803**	**System on Chip Design**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers SoC design and modeling techniques with emphasis on architectural exploration, assertion-driven design and the concurrent development of hardware and embedded software.	
Module 1	**Low-level modeling and design refactoring**	12 hours
Verilog RTL Design with examples. Simulation styles (fluid flow versus eventing). Basic RTL to gates synthesis algorithm. Using signals, variables and transactions for component inter-communication. SystemC overview. Structural hazards, retiming, refactoring.		
Module 2	**Design partition, high-level and hybrid modeling**	12 hours
Bus and cache structures, DRAM interface. SoC parts. Design exploration. Hardware/software interfaces and co-design. Memory maps. Programmer's model. Firmware development. Transactional modeling. Electronic systems level (ESL). IP-XACT. Instruction set simulators, cache modeling and hybrid models.		
Module 3	**Assertions for design, testing and synthesis**	10 hours
Assertion based design: testing and synthesis. PSL/SVA assertions. Temporal logic compilation to FSM. Glue logic synthesis. Combinational and sequential equivalence. High- level Synthesis and Automated Assembly.		
Module 4	**Power control and power modeling**	8 hours
Power consumption formulae. Pre-layout wiring estimates. Clock gating. Frequency and voltage dynamic scaling.		

Reference Books

1. Lin, Y-L.S. *Essential issues in SOC design: designing complex systems-on-chip*, Springer, 2006.
2. Grotker, T., Liao, S., Martin, G. & Swan, S. *System design with SystemC*, Springer, 2002.
3. Ghenassia, F. *Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems*, Springer, 2010.
4. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, *Embedded System Design: Modeling, Synthesis, Verification*, Springer, 2009.
5. G. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994.

Subject Code **EC804**	**Mixed Signal Design**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers theory and concepts to Integrate both Analog and Digital subsystems on a single monolithic chip to create an electronic system. The syllabus includes primitive cells, biasing and references, op-amp designs, switched capacitor A/D and D/A converters, and clock generation systems for digital and mixed signal.	
Module 1	**Filter basics**	10 hours
Analog continuous-time filters: passive and active filters, Basics of analog discrete-time filters and Z-transform, Sample and Hold Circuits, Switched-capacitor filter architectures.		
Module 2	**ADC and DAC**	12 hours
Basics ADC, Successive approximation ADCs, Flash ADC, folding-and-interpolation ADC, Pipeline ADC, Introduction/Characterization of DACs, various architectures of high speed DAC		
Module 3	**Over sampled ADC**	10 hours
Over sampled ADC: Working principle and architecture of a Sigma-delta ADC, multistage sigma-delta converters, Design of decimation filter.		
Module 4	**Advanced Topics**	10 hours
VCO, Loop Filter, Charge pump, Precautionary measures for integrating analog and digital modules within an IC, floor planning and physical design of mixed signal IC design.		

Reference Books

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education, 2002.
2. David Johns & Ken Martin, *Analog Integrated Circuit Design*, Wiley-India, 2008.
3. P. Allen & D. R. Holberg, *CMOS Analog Circuit Design*, Oxford Press, 2011.
4. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
5. Schreier & Temes, *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press, 2004.
6. Franco Maloberti, *Data Converters*, Springer-2007.
7. Jacob Baker, *CMOS Mixed Signal Circuit Design*, Wiley-IEEE Press, Second Edition, 2009.

Subject Code **EC805**	**VLSI & Embedded systems**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	The course covers prototype development of embedded VLSI system. The course focuses on software application by mapping of functions onto hardware components. In addition to the conceptual foundations, this course also covers various design methodologies and platforms based on ARM and FPGA.	
Module 1	**Embedded System on chip platforms**	5 hours
Introduction to embedded system and design methodology for ARM and FPGA devices, Prototype development of embedded application advantages, design challenges, Differences between General Purpose Processor, Digital signal Processor, ASIC and FPGA based System On Chip.		
Module 2	**MPSoC platform for FPGAs and ARM**	25 hours
Embedded Computer Organization, emphasis on different embedded processors and multiprocessor and architectures. Application profiling, Hardware-software co-design, Simple & Autonomous I/O Controllers, Custom IP (Intellectual-Property) hardware design for System-On-a-Chip; Design of Master and Slave Bus protocols based IPs, Bus protocols (AXI, PLB, FSL, NPI etc.). Concepts & types of Memory and interfacing, Cache Memory, Cache mapping techniques and impact on system performance, Design Metrics, General purpose peripherals (interrupt, timer, clock, DMA etc.) and special purpose peripherals Serial Transmission techniques & Standards, Wireless protocols, and advanced high speed buses.		
Module 3	**Analysis and case-studies**	12 hours
Architecture exploration of IP, System Level Design Trade-offs, Power, Energy, Performance and Area. Frequency, memory and power, Productivity, Reusability, Clocking and Synchronisation issues, Co-simulation using different simulators, system level optimization, Design for Test, Advanced design Methodologies using HLS for an application like JPEG 2000, MJPEG, H.264, Embedded operating systems for SoC platforms.		

Reference Books

1. Ron Sass and Andrew G. Schmidt, *Embedded Systems Design with Platform FPGAs Principles and Practices*, Elsevier Inc, 2010.
2. Doug Amos, Austin Lesea and Rene Richter, *FPGA-Based Prototyping Methodology Manual Best Practices in Design-for-Prototyping*, Synopsys, Inc, Mountain View, 2010.
3. *Embedded System Design: A unified Hardware/Software Introduction*, Frank Vahid, and Tony Givargis.
4. Lin, Y.L.S., *Essential issues in SOC design: designing complex systems-on-chip*, Springer, 2006.
5. Sloss, Andrew, Dominic Symes, and Chris Wright, *ARM system developer's guide: designing and optimizing system software*. Morgan Kaufmann, 2004.
6. G. DeMicheli, R. Ernst, and W. Wolf, *Readings in Hardware/Software Co-Design*, Academic Press, 2002.
7. Peter J. Ashenden, *Digital Design: An Embedded Systems Approach Using Verilog*, Morgan Kaufmann Publication, 2008.

Subject Code **EC806**	**VLSI Design Automation**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	The objective of physical design automation is to carry out mapping of the given structural representation into layout representation optimally using computers so that the resulting layout satisfies topological, geometric, timing and power-consumption constraints of the design.	
Module 1	**VLSI CAD basics**	12 hours
VLSI CAD Flow, Chip Layout styles, High-level synthesis, Algorithm Design Approaches for VLSI CAD, models for physical design, Graph theory fundamentals.		
Module 2	**Partitioning and Routing**	12 hours
Partitioning, Floorplanning-tutte's approach, Graph-theoretic models of floorplans, Placement-general problem, quality metrics, Gordian, Design Rule Check, Compaction, Clock and Power Routing–Global routing, Channel routing.		
Module 3	**Optimization and Synthesis**	10 hours
Optimization techniques, Logic synthesis and Technology Mapping-Dynamic Programming, Dagon, VLSI and Circuit Design Issues including power and delay analysis.		
Module 4	**New topics in VLSI CAD**	8 hours
Design consideration for Analog and Mixed Signal Design. Emerging topics in the VLSI CAD.		

Reference Books

1. S. M. Sait, and H. Youssef, *VLSI Physical Design Automation: Theory and Practice*, World Scientific, 1999.
2. T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms*, MIT Press, Third Edition, 2009.
3. C. J. Alpert, D. P. Mehta, S. S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, Auerbach Publications, 2008.
4. Sung Kyu Lim, *Practical Problems in VLSI Physical Design Automation*, Springer, 2008.
5. Naveed A Sherwani, *Algorithms for VLSI Physical Design Automation*, Third Edition, 1998.

Subject Code **EC807**	**Compound Semiconductor Devices**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	The goal of this course is to impart the elements of III-V compound semiconductor materials and their related electronic and photonic devices.	
Module 1	**Introduction to compound semiconductor**	12 hours
Compound semiconductor crystals, structural, optical properties and electrical properties, free carrier concentration and Fermi-Dirac integral, III-V alloys, Fermi level pinning, theories of barrier formation and of current flow, diffusive vs. ballistic flow; contrasts with p-n diodes.		
Module 2	**Heterostructures**	12 hours
E-x Profiles, modulation doping. Conduction parallel to heterojunction; mobility in semiconductors and carrier scattering mechanisms, Conduction normal to junction: I-V models and characteristics.		
Module 3	**MESFETs**	10 hours
Basic concept, models for terminal characteristics; accounting for velocity saturation. Dynamic models: large signal switching transients; small signal, high f models. Fabrication sequences; application-specific designs, examples of fabrication sequences.		
Module 4	**HFETs & HBTs**	8 hours
Basic device, theory, Deep level problem, non-ideal behaviour, pseudomorphic solution, RF characteristics,.		
Reference Books 1. M. S. Shur, M. S, *Physics of Semiconductor Devices*, Prentice-Hall, 1990. 2. Adachi, Sadao, *Physical Properties of III-V Semiconductor Compounds: InP, InAs, GaAs, GaP, InGaAs, and InGaAsP*, John Wiley & Sons, 1992. 3. S. M. Sze, High *Speed Semiconductor Devices,* Wiley, 1990. 4. S. M. Sze, *Physics of Semiconductor Devices*, Wiley, Second Edition, 1981.		

Subject Code **EC808**	**Nano-Electronic Device Engineering**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course will introduce the rapidly developing field of nano-engineering materials and various device structures with special focus on their electronic properties.	
Module 1	**Device Physics and Introduction to scaling issues**	12 hours
Challenges going to sub-100 nm MOSFETs – fundamental limits for MOS operation, SCEs and DIBL effects, sub-threshold current, velocity saturation, Oxide layer thickness, tunneling, High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance, power density, non-uniform dopant concentration,. interconnect and lithography issues.		
Module 2	**Novel Device Structures**	12 hours
Novel MOS-based devices – Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices. SiGe HBTs.		
Module 3	**Hetero structure based devices**	10 hours
Hetero structure based devices – Type I, II and III Heterojunction, Si-Ge heterostructure, hetero structures of III-V and II-VI compounds - resonant tunneling devices, MODFET/HEMT, Carbon nanotubes based devices – CNFET, characteristics, Spin-based devices – spinFET, characteristics.		
Module 4	**Quantum Effects**	8 hours
Quantum structures – quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations		

Reference Books

1. Mircea Dragoman and Daniela Dragoman, *Nanoelectronics – Principles & devices*, Artech House Publishers, 2005.
2. Karl Goser, Nanoelectronics and Nanosystems: *From Transistors to Molecular and Quantum Devices*, Springer 2005.
3. Mark Lundstrom and Jing Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*, Springer, 2005.
4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, *Quantum heterostructures*, Cambridge University Press, 1999.
5. S. M. Sze (Ed), *High speed semiconductor devices*, Wiley, 1990.
6. H.R. Huff and D.C. Gilmer, *High Dielectric Constant Materials for VLSI MOSFET Applications*, Springer 2005.
7. B. R. Nag, *Physics of Quantum Well Devices*, Springer 2002.
8. E. Kasper, D. J. Paul, *Silicon Quantum Integrated Circuits Silicon-Germanium Heterostructures Devices: Basics and Realisations*, Springer, 2005.

Subject Code **EC809**	**Active Filter Design**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	To understand the fundamental concepts involved in the design of Continuous-time filters. To develop the skills required to design and verify the various filter circuits using op-amps and OTA's.	
Module 1	**Filter Fundamentals**	10 hours
Filter Characterization, Continuous-Time Filter Functions, Steps in Filter design, Butterworth, Chebyshev & Inverse-Chebyshev filter response and pole locations. The Approximation Problem.		
Module 2	**Ladder filter structures**	10 hours
LC ladder filter - prototype & synthesis; Frequency transformation of low-pass filter. Active elements , Impedance converters, Characteristics of IC op-amps , The Ideal Operational Transconductance Amplifier (OTA).		
Module 3	**Realizations of active filters**	12 hours
Active-RC filters, Gm-C filters- Elementary Transconductance Building blocks, off-set problems, Limitations of opamp based filters. Characterization of on-chip integrated continuous time filters.		
Module 4	**Switched capacitor circuits**	10 hours
Switched capacitor filters- First-order building blocks- Second order sections.		

Reference Books

1. R. Schaumann and M.E. Van Valkenburg, *Design of Analog Filters*, Oxford University Press, 2003.
2. P. V. Ananda Mohan, *Current-Mode VLSI Analog Filters - Design and Applications*, Birkhauser, 2003.
3. Gobind Daryanani, *Properties of Active networks synthesis and Design*, Wiley, First Edition, 1976.
4. M.E. Van Valkenburg, *Analog Filter Design*, Oxford University Press, 1995.
5. T. Deliyannis, Y. Sun and J. K. Fidler, *Continuous-Time Active Filter Design*, CRC Press, 1998.
6. Material from the Journal of Solid-state Circuits and the International Solid-state Circuits Conference proceedings.

Subject Code **EC810**	**Low-Power VLSI Design**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	To understand the critical requirements and implementation of Low-power VLSI circuits. The course also covers critical issue related to continued scaling of microelectronic circuits.	
Module 1	**Introduction**	08 hours
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits, Emerging Low power approaches. Device & Technology Impact on Low Power: short circuit and leakage in CMOS, Dynamic dissipation in CMOS.		
Module 2	**Low-Voltage CMOS Circuits**	10 hours
Introduction, Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect, Low voltage design techniques using reverse Vgs, steep sub threshold swing and multiple threshold voltages, Testing with elevated intrinsic leakage, multiple supply voltages.		
Module 3	**Circuit and logics**	12 hours
Low Power Circuits: Transistor and gate sizing, network restructuring and Reorganization, Special Flip Flops & Latches design, Low power digital cells library. Logic level- Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.		
Module 4	**Architecture and system**	12 hours
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components. Adiabatic Computation, Pass Transistor Logic Synthesis.		

Reference Books

1. Gary K. Yeap, *Practical Low Power Digital VLSI Design*, KAP, 2002
2. Kaushik Roy, and Sharat Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.
3. Anantha P. Chandrakasan, and Robert W. Brodersen, *Low Power Digital CMOS Design*, Kluwer Academic Publications, 1995.
4. Rabaey, and Pedram, *Low Power Design Methodologies*, Kluwer Academic,1997
5. Philip Allen, and Douglas Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2002.

Subject Code **EC811**	**Power Management ICs**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers operation principles of different dc-dc converters: switched-mode power converters, switched-capacitor power converters and linear regulators. Design and analysis of voltage references are also covered.	
Module 1		12 hours
Introduction to DC to DC converter, Mechanisms of switching loss, Switching in Inductor, Buck converter, Synchronous Buck converter, Boost converter, Cuk Converter, dc-ac inverters, Small-signal ac modeling, and analysis of various DC to DC converters.		
Module 2		12 hours
Single ended primary inductance converter, interleaved converters, PWM building blocks, Various control techniques, PWM control of DC-DC converter, Stabilization.		
Module 3		8 hours
Zero current switching DC-DC converters, Zero Voltage switching DC-DC converter, ZVS converter, flyback converter, resonant converters, PWM for Class D audio amplifier.		
Module 4		10 hours
Voltage references, Temperature and power supply sensitivity, Analysis of negative feedback circuits, voltage regulators. Applications emphasized include dc-dc converters for computer power and portable applications, dc-ac inverters for gas discharge lighting ballasts and wireless power transfer, LED drivers and solar micro-inverters.		
Reference Books 1. Gabriel Rincon-Mora, *Analog IC Design with Low Dropout Regulators*, McGraw-Hill, 2009. 2. Marian K. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*, Wiley, 2008. 3. R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Kluwer, Second Edition, 2001.		

Subject Code **EC812**	**Advanced Topics in VLSI**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the advanced topics in the VLSI Design and emphasis will be given to one specific domain of integrated circuit design. Most often, this will address an application space that has become particularly relevant in recent times. Examples are serial links, ultra-low-power design, wireless transceiver design.	
Module 1		21 hours
Topics on Wireless transceiver design, Sensor design, Wireless body area networks, RF ID		
Module 2		21 hours
Topics on Ultra low power design, Serial links etc.		
References 1. Journal of Solid-State Circuits (JSSC) 2. Transactions of Circuits and Systems I (TCAS-I) 3. Transactions of Circuits and Systems II (TCAS-II) 4. Transactions on Very Large Scale Integration Systems (TVLSI) 5. IEEE Journal on Emerging and Selected Topics in Circuits and Systems 6. Other relevant Journal and conference papers		

Subject Code **EC813**	**Memory Design & Testing**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the analysis, design and testing of Memory Circuits starting from basic building blocks. Memory technologies like DRAM, SRAM, FLASH and interfacing circuits are covered.	
Module 1		12 hours
Review of CMOS circuit design, architectures, Open and folded arrays, sensing basics, refresh, kickback, SRAM (Read and Write operation, 6T, 8T cell implementation etc.), floating-gate architectures, sense amplifiers, Sensing using Sigma-Delta Modulation.		
Module 2		12 hours
Introduction to DRAM, High speed DRAM architectures, bandwidth, latency, and cycle time, Power, Timing circuits, Control logic, FLASH (FLASH array sensing and programming), Charge Pump, PROM, EPROM		
Module 3		10 hours
RAM Fault Modeling, RAM Electrical Testing, RAM Pseudorandom Testing, Megabit DRAM Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing. General Design for Testability Techniques, RAM Built-in Self-Test (BIST), Embedded Memory DFT and BIST Techniques, Advanced BIST and Built-in Self-Repair Architectures. DFT and BIST for ROMs, Memory Error-Detection and Correction Techniques, Memory Fault-Tolerance Designs.		
Module 4		8 hours
Reliabilities issues, Topics in Advanced Memory Technology, Application Specific Memories and Architectures, High Density memory package Technologies.		
Reference Books 1. Betty Prince, *Semiconductor Memories: A Handbook of Design, Manufacture and Application*, Wiley, Second Edition, 1996. 2. Keeth, Baker, Johnson, and Lin, *DRAM Circuit Design: Fundamental and High-Speed Topics*, Wiley-IEEE, 2007. 3. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, Wiley-IEEE, Third Edition, 2010. 4. Ashok K. Sharma, *Semiconductor Memories: Technology, Testing, and Reliability*, Wiley-IEEE, 2013.		

Subject Code **EC814**	**IC for Broadband communication**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	The objective of this course is to study digital signal transmission over lossy and dispersive channels, equalization, IC broadband amplifiers, feed-forward and decision feedback equalization, clock and data recovery circuits. It provides an understanding of signal degradation, techniques to combat them, and integrated circuit implementation of these techniques.	
Module 1	**Digital signal transmission**	12 hours
Digital signal transmission over lossy and dispersive channels: Eye diagrams; Eye closure; crosstalk, and jitter; Synchronization: clock and data recovery circuits using phase locked loops and delay locked loops,		
Module 2	**Equalization**	12 hours
Equalization: Transmit pre-emphasis, Receive feed-forward equalization, and decision feedback equalization.		
Module 3	**IC broadband amplifiers for transmitter and receiver**	10 hours
Integrated circuit implementation of broadband amplifiers for transmission and reception, feed-forward and decision feedback equalization.		
Module 4	**Clock and data recovery circuits**	8 hours
Clock and data recovery circuits, multiplexers, and demultiplexers.		

Reference Books

1. David Johns and Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.
2. Y. Tsividis, *Mixed Analog Digital VLSI Devices and Technology (An introduction*), World Scientific, 2002.
3. Gray, Hurst, Lewis, and Meyer, *Analysis and design of Analog Integrated Circuits*, John Wiley and Sons, Fifth Edition, 2009.
4. K. R. Laker and W.M.C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994.
5. Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2000.

Subject Code **EC815**	**CMOS RF IC Design**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	The objective of this course is to cover the circuit design theory and their implementation techniques at RF frequencies specific to CMOS technologies.	
Module 1	**Historical Aspects**	8 hours
Historical Aspects — From Maxwell to current wireless standards, The bridge between communication system designer and RF IC designer, common system characterization, RF system characterization.		
Module 2	**Transceiver Architectures**	8 hours
Transceiver Architectures — motivation for the individual blocks, lumped, passive RLC, RF properties of MOS, Tuned amplifiers.		
Module 3	**Low Noise Amplifier and mixer**	14 hours
Noise sources, cascades, Low Noise Amplifier — design examples, Mixers — Introduction, active and passive.		
Module 4	**Oscillators & synthesizers**	12 hours
Analysis fundamentals and inductors, LC oscillators and VCOs, Frequency Synthesizers: Principles, design, Integer N vs. Fractional PLL.		

Reference Books:

1. T. H. Lee, *The Design of Radio-Frequency Integrated Circuits*, Cambridge University Press, 2004.
2. B. Leunge, *VLSI for Wireless Communication, Personal Education Electronics and VLSI series*, Pearson Education, 2002.
3. B. Razavi, *RF Microelectronics*, Prentice Hall, 1998.

Subject Code **EC816**	**Advanced Antenna Theory**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	The main objective is to study modern antenna concepts for various applications. The course will explain basic antenna parameters, different types of antenna and array configurations. The concepts can further be extended in the VLSI domain for RF IC design.	
Module 1	**Fundamental Concepts**	10 hours
Physical concept of radiation, Radiation pattern, near-and far-field regions, reciprocity, directivity and gain, effective aperture, polarization, input impedance, efficiency.		
Module 2	**Radiation from Wires and Loops.**	10 hours
Infinitesimal dipole, finite-length dipole, linear elements near conductors, dipoles for mobile communication, small circular loop.		
Module 3	**Aperture, Reflector and Broadband Antennas.**	12 hours
Huygens' principle, radiation from rectangular and circular apertures, radiation from sectoral and pyramidal horns, prime-focus parabolic reflector antennas, Log-periodic and Yagi antennas, frequency independent antennas, broadcast antennas.		
Module 4	**Microstrip Antennas and Antenna Arrays**	10 hours
Basic characteristics of microstrip antennas, feeding methods, methods of analysis, design of rectangular and circular patch antennas, Analysis of uniformly spaced arrays with uniform and non-uniform excitation amplitudes.		
Reference Books 1. C. A. Balanis, *Antenna Theory and Design,* John Wiley & Sons, Third Edition, 2005. 2. W. L. Stutzman, and G. A. Thiele, *Antenna Theory and Design,* John Wiley & Sons, Second Edition, 1998. 3. R. S. Elliot, *Antenna Theory and Design,* Wiley-IEEE Press, Revised Edition, 2003.		

Subject Code **EC817**	**VLSI Signal Processing**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the various VLSI architectures and algorithms for digital signal processing. This course describes the basic ideas about digital signal processing. This course also describes the techniques of critical path and algorithmic strength reduction in the filter structures.	
Module 1	**DSP Concepts**	12 hours
Linear system theory, DFT, FFT, realization of digital filters. Typical DSP algorithms, DSP applications. Data flow graph representation of DSP algorithm.		
Module 2	**Architectural Issues**	10 hours
Binary Adders, Binary multipliers, Multiply Accumulator (MAC) and Sum of Product (SOP). Pipelining and Parallel Processing, Retiming, Unfolding, Folding and Systolic architecture design.		
Module 3	**Fast Convolution**	10 hours
Cook-Toom algorithm, modified Cook-Toom algorithm, Winograd algorithm, modified Winograd algorithm, Algorithmic strength reduction in filters and transforms, DCT and inverse DCT, parallel FIR filters.		
Module 4	**Power Analysis in DSP systems**	10 hours
Scaling versus power consumption, power analysis, power reduction techniques, power estimation techniques, low power IIR filter design, Low power CMOS lattice IIR filter.		

Reference Books

1. Keshap K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, John Wiley, 2007.
2. U. Meyer-Baese, *Digital Signal processing with Field Programmable Arrays*, Springer, 2007.
3. V. K. Madisetti, *VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis*, IEEE Press, New York, 1995.
4. S. Y. Kung, H. J. Whitehouse, *VLSI and Modern Signal Processing*, Prentice Hall, 1985.

Subject Code **EC818**	**Multi-rate Signal Processing**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the basic ideas about decimator, interpolator, multi-rate filter design and DFT filter banks. This course also describes the design of filter bank and efficient implementation of the filter banks.	
Module 1	**Introduction**	10 hours
Introduction, Sampling and Signal Reconstruction, Sampling rate conversion, Decimation by an integer factor, Interpolation by an integer factor, Sampling rate conversion by a rational factor, Sampling rate converter as a time variant system, Practical structures for decimators and interpolators.		
Module 2	**Multi-rate filter design**	10 hours
Direct form and Polyphase FIR structures, FIR structures with time varying Coefficients, Design of FIR filters for sampling rate conversion, Multistage design of decimator and interpolator, Applications of Interpolation and decimation in signal processing.		
Module 3	**Maximally Decimated Filter Banks**	10 hours
Introduction, errors created in QMF bank, alias free QMF system, power symmetric QMF banks, M-channel filter banks, polyphase representation, perfect reconstruction systems; Paraunitary Perfect Reconstruction (PR) Filter Banks, lossless transfer matrices, filter bank properties induced by paraunitariness, two channel FIR paraunitary QMF banks, two channel paraunitary QMF lattice, M-channel FIR paraunitary filter banks;		
Module 4	**Linear Phase Perfect Reconstruction QMF Banks**	12 hours
Introduction, lattice structures for linear phase FIR PR QMF banks, formal synthesis of linear phase FIR PR QMF lattice; Cosine modulated Filter Banks, efficient polyphase structures, cosine modulated perfect reconstruction systems. Applications of Multirate Signal Processing: Analysis of audio, speech, image and video signals.		
Reference Books 1. P. P. Vaidyanathan, *Multirate Systems and Filter Banks*, Pearson-Education, 2004. 2. N. J. Fliege N J, *Multirate Digital Signal Processing*, John Wiley and sons, 1994. 3. J. G. Proakis, & D. G. Manolakis, *Digital Signal Processing Principles, Algorithms and Applications*, Prentice Hall of India, 2002. 4. S. K. Mitra, *Digital Signal Processing-A Computer Based Approach*, Tata McGraw Hill, 2003.		

Subject Code **EC819**	**Multimedia-Systems**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	The objective of the course is to learn hardware accelerators for various modules in embedded systems. The course covers basics of embedded multimedia, image processing systems and various algorithms for multimedia and image processing.	
Module 1	**Multimedia Application**	5 hours
An extensive overview of state-of-the-art techniques, traditional development flows and algorithms on multimedia, image and multimedia processing, audio processing and highlight their limitations in the light of performance, power, and memory requirements. Programmable and custom architectures and algorithms, advanced video memories hierarchies and specialized (multi-/many-core) hardware processor architectures and design methods (e.g., Pipelined MPSoCs, Stream Processors, and Stochastic Processors).		
Module 2	**Algorithms and Embedded systems**	17 hours
Review of various architecture types, design consideration, memory reuse mechanisms, sub-task scheduling, architecture evaluation, resource sharing; High performance architectures, wavelet VLSI architectures; DCT architectures; lossless coders, Advanced arithmetic architectures and design methodologies: division and square root; finite field arithmetic; cordic algorithms and architectures for fast and efficient vector-rotation implementation; advanced systolic design; low power design; power estimation approaches; system exploration for custom low power data storage and transfer; hardware description and synthesis of DSP systems.		
Module 3	**Architectures for multimedia CODEC module**	20 hours
Design and analysis of several light-weight multimedia and image processing algorithms and computation management techniques. Study of various architectures for motion estimation, Intra prediction, Integer discrete cosine transform, motion compensation , deblocking filter, entropy coder, system integration and Future generation hardware codecs.		

Reference Books

1. Richardson, Iain E, *The H.264 advanced video compression standard*, John Wiley & Sons, 2011.
2. Articles on IEEE Transactions on Circuits and Systems for Video Technology, Multimedia, VLSI Systems, consumer electronics etc.,.
3. Lee, Jae-Beom, and Hari Kalva. *The VC-1 and H. 264 video compression standards for broadband video services*. Vol. 32, Springer, 2008
4. Parhi, Keshab K., and Takao Nishitami, *Digital signal processing for multimedia systems*, CRC Press, 1999.
5. Parhi, Keshab K, *VLSI digital signal processing systems: design and implementation*, John Wiley & Sons, 2007.
6. Tian, Xiaohua, M. Le Thinh, and Yong Lian, *Entropy Coders of the H. 264/AVC Standard*, Springer, 2011.
7. Lin, Youn-Long Steve, et al. *VLSI Design for Video Coding*, Springer, 2010.
8. Ramachandran, and Seetharaman, *Digital VLSI systems design*, springer, 2007.

Subject Code **EC820**	**Selected Topics in ECE-I**	Credits: 1 Total hours: 14
Course Objectives	This course covers the current topics in the ECE and emphasis will be given to application space that has become particularly relevant in recent times.	
Syllabus can be framed according to the need.		

Subject Code **EC821**	**Selected Topics in ECE-II**	Credits: 2 Total hours: 28
Course Objectives	This course covers the current topics in the ECE and emphasis will be given to application space that has become particularly relevant in recent times.	
Syllabus can be framed according to the need.		

Subject Code **EC822**	**Selected Topics in ECE-III**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	This course covers the current topics in the ECE and emphasis will be given to application space that has become particularly relevant in recent times.	
Syllabus can be framed according to the need.		

Program Electives

Subject Code **EC850**	**Data Structures & Algorithms**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	Following this course, students will be able to: 1) Solve problems using data structures such as linear lists, stacks, queues, hash tables, binary trees, heaps, tournament trees, binary search trees, and graphs and writing programs for these solutions. 2) Solve problems using algorithm design methods such as the greedy method, divide and conquer, dynamic programming, backtracking, branch and bound and writing programs for these solutions.	
Module 1		4 hours
Introduction to data structures and objectives, basic concepts Arrays: one dimensional, multi-dimensional, Elementary Operations.		
Module 2		6 hours
Stacks: Representation, elementary operations and applications such as infix to postfix, postfix evaluation, parenthesis matching, Queues: Simple queue, circular queue, dequeue, elementary operations and applications.		
Module 3		8 hours
Linked lists: Linear, circular and doubly linked lists, elementary operations and applications such as polynomial manipulation.		
Module 4		8 hours
Trees: Binary tree representation, tree traversal, complete binary tree, heap, binary search tree, height balanced trees like AVL tree and 2-3 tree and other operations and applications of trees.		
Module 5		8 hours
Graphs: Representation, adjacency list, graph traversal, path matrix, spanning tree; introduction to algorithm analysis and design techniques, algorithms on sorting: selection sort, bubble sort, quick sort, merge sort, heap sort, searching, linear and binary search.		
Module 6	**(Miscellaneous Topics)**	10 hours
Hash tables, direct address tables, hash tables, hash functions, open addressing, search trees , binary search trees, red-black Trees, splay trees. B – Trees, binomial heaps, fibonacci heaps, data structures for disjoint sets. Suffix Trees-Tries-Text compression, text similarity testing-range trees, priority search trees, quad trees and k-d trees.		
Reference books 1. Alfred V Aho, John E Hopcroft, Jeffrey D. Ullman, *Data structures & algorithms*, Addison Wesley, 2003. 2. Ellis Horowitz, Sartaj Sahni and Dinesh Mehta, *Fundamentals of data structures and algorithms using C++*, Galgotia Publications, Second Edition, 2006. 3. Michael T. Goodrich, Roberto Tamassia, *Data Structures and algorithms in Java*, John Wiley & Sons, Inc., Fourth Edition, 2010. 4. Thomas H. Cormen, Charles E. Leiserson, Ronald L.Rivest, Clifford Stein, *Introduction to algorithms*, MIT Press, Second Edition, 2003.		

Subject Code **EC851**	**Advanced Computer Architecture**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	The objective of the course is to cover concepts related to parallel computer models, advanced processors, pipelining, multiprocessors, and memory hierarchy design for optimal performance of the system.	
Module 1	**Parallel Computer Models**	10 hours
Classification of parallel computers, multiprocessors and multicomputer, conditions of parallelism, data and resource dependencies, grain size and latency, grain packing and scheduling, program flow mechanisms, system interconnect architectures.		
Module 2	**Advanced Processors**	12 hours
Principles of scalable performance, performance metrics and measures, superscaler and vector processors, advanced processor technology, CISC scalar processors, RISC scalar processors, superscalar processors, VLIW architectures, vector and symbolic processors.		
Module 3	**Pipelining and Multiprocessors**	12 hours
Linear pipeline processor, nonlinear pipeline processor, instruction pipeline design, mechanisms for instruction pipelining, dynamic instruction scheduling, branch handling techniques, branch prediction, arithmetic pipeline design, multifunctional arithmetic pipelines, Multiprocessors and multi computers, multiprocessor system interconnects, cache coherence and synchronization mechanisms, message passing schemes.		
Module 4	**Memory Hierarchy Design**	8 hours
Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.		

Reference Books:

1. K. Hwang, *Advanced Computer Architecture*, TMH, 2001.
2. W. Stallings, *Computer Organization and Architecture*, McMillan, 1990.
3. M. J. Quinn, *Designing Efficient Algorithms for Parallel Computer*, McGraw Hill, 1994.

Subject Code **EC852**	**Optimization Techniques**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	The objective of this course is to study convex optimization techniques, non-linear programming with unconstrained and constrained optimization problems, reliability theory and dynamic programming.	
Module 1	**Convex optimization techniques**	12 hours
Convex sets and functions, constrained optimization methods: Introduction, Kuhn-Tucker conditions, convex optimization, Lagrange multipliers.		
Module 2	**Non-linear programming**	8 hours
One-dimensional minimization method, search method, unconstrained and constrained optimization theory and practices.		
Module 3	**Reliability**	10 hours
Basic concepts, conditional failure rate function, Failure time distributions, Certain life models, Reliability of a system in terms of the reliability of its components, series system, and Parallel system.		
Module 4	**Dynamic Programming**	12hours
Multistage decision problems, computation procedure and case studies. Fundamentals of queuing system, Poisson process, the birth and death process, special queuing methods.		

Reference Books:

1. S. S. Rao, *Optimization: Theory and Practices*, New Age Int. (P) Ltd. Publishers, 2009.
2. E. K. P. Chong, and S. H. Zak, *An Introduction to Optimization*, John Wiley & Sons, 2013.
3. A. L. Peressimi, F. E. Sullivan, J. J. Uhl, *Mathematics of Non-linear Programming*, Springer Verlag, 1993.

Subject Code **EC853**	**Linear Algebra**	Credits: 3 (3-0-0) Total hours: 42
Course Objectives	This course covers the fundamentals of linear algebra and matrices theory. It is intended as a broad course from engineering perspective. The first part covers the vector space, transformations and matrices theory and also provides the geometrical setting. The second part is intended to solve practical problems and provide algorithmic solutions.	
Module 1	**Vector Space**	5 hours
Vector Spaces, vector algebra, subspaces, basis vectors, Linear Transformations and Matrices, matrix rank, matrix norms, determinant, inverse, condition number;		
Module 2	**Characteristic Equation**	5 hours
Eigen values and vectors of matrices and eigenvalue decomposition; Hermitian and symmetric matrices, positive definite matrices, unitary matrices, projection matrices and other special matrices;		
Module 3	**Inner Product Space**	5 hours
Inner product spaces and vector norms, Gramm-Schmidt orthonormalization; bilinear forms;		
Module 4	**Solution of Equations**	5 hours
Solution of equations: Gaussian Elimination, pivoting, LU and Cholesky factorizations;		
Module 5	**Orthogonolization**	7 hours
Orthogonalization and Least Squares: Householder and Givens Matrices, QR factorizations, Full Rank Least Squares(LS) Problem, Rank Deficient LS Problem;		
Module 6	**Eigen Value Problem**	8 hours
Symmetric Eigenvalue Problem: power iterations, symmetric QR algorithm, Jacobi methods, tridiagonal methods, SVD, Lanczos and Arnoldi methods;		
Module 7	**Iterative Methods**	7 hours
Iterative Methods for Linear Systems: Jacobi and Gauss-Seidel iterations, SOR methods;		

Reference Books

1. Golub and Van Loan, *Matrix Computations*, Johns Hopkins University Press, Thrid Edition, 1996.
2. Strang, *Linear Algebra and its Application*, Cengage Learning, Fourth edition, 2005.
3. Horn and Johnson, *Matrix Analysis*, Cambridge University Press, 1990.
4. Hoffman and Kunze, *Linear Algebra*, Prentice Hall, Second Edition, 2009.

Subject Code **EC854**	**Random Processes**	Credits: 3(3-0-0) Total hours: 42
Course Objectives	This course covers the foundations and major concepts in random processes which are required for communications and signal processing concepts.	
Module 1	**Preliminaries**	8 hours
Axioms of Probability, Independence and Conditional Probability, Random Variables and their Distribution, Functions of Random Variables, Expectation, Frequently used Distributions, Jointly Distributed Random Variables, Cross Moments, Conditional Densities,		
Module 2	**Convergence of Sequence of Random Variables**	10 hours
Various types of Convergence, Cauchy Criteria for Convergence, Limit Theorems, Convex Functions and Jensen's Inequality, Chernoff Bound and Large Deviation Theory.		
Module 3	**Random Vectors and MMSE Estimation**	10 hours
Basic Definitions, The Orthogonality Principle of MMSE Estimation, Gaussian Random Vectors, Linear Innovations Sequences, Discrete Time Kalman Filtering		
Module 4	**Random Processes**	14 hours
Random Processes, Stationarity, Counting Processes and Poisson Process, Markov Process, Discrete Time Markov Chain, Continuous Time Markov Chain, Renewal Theory, Introduction to Martingales.		

Reference Books

1. Bruce Hajek, *An Exploration of Random Processes for Engineers*, Class Notes, 2014.
2. Sheldon Ross, *Stochastic Processes*, John Wiley and Sons, 1996.
3. Dimitri Bertsekas, John Tsitsiklis, *Introduction to Probability*, Athena Scientific, First Edition, 2002.
4. A Papoulis, S. U. Pillai, *Probability, Random Variables and Stochastic Processes*, Tata McGraw-Hill, Fourth Edition, 2002.